CLAIMS

What is claimed is:

1. A single integrated circuit comprising

a plurality of logic elements (LEs) for generating a plurality of output signals in response to a plurality of input signals correspondingly applied to the LEs, each of the LEs being equipped to hold constant the LE's output signal on demand; and

a context bus, including associated read/write control facilities, coupled to the LEs for outputting individual signal state values of the LEs out of the integrated circuit, and for initializing the LEs with individual signal state values provided to the integrated circuit while the output signals of the LEs are being held constant.

2. The integrated circuit as set forth in claim 1, wherein the integrated circuit further comprises a scan register coupled to the LEs for serially capturing and outputting a trace record of all signal state values of the LEs in a particular clock cycle of an operating clock outside the integrated circuit, the scan register being provided with a scan clock appropriately scaled to the operating clock.

3. The integrated circuit as set forth in claim 1, wherein the integrated circuit further comprises trigger circuitry coupled to the LEs for conditionally generating at least one trigger value depending on the signal state values of the LEs.

4. The integrated circuit as set forth in claim 3, wherein the trigger circuitry comprises

a first register for storing a first trigger pattern; and

a first comparator coupled to the LEs and the first register for conditionally generating a first trigger value if signal state values of the LEs match the stored first trigger pattern.

5. The integrated circuit as set forth in claim 1, wherein

each LE further includes a multiple input-single output truth table for generating a first intermediate output signal in response to a first set of input signals;

a first selector coupled to the truth table and the context bus for selecting either the first intermediate output signal, the output of the LE fedback to the first selector, or a predesignated bus signal on the context bus, and outputting the selected signal; and

a first control circuit coupled to the first selector for controlling the first selector.

6. The integrated circuit as set forth in claims 5, wherein each LE further comprises

a pair of master-slave latches, each having a data input, a set input, and a reset input, coupled to the first selector for generating a second and a third intermediate output signal in response to the data, set, and reset inputs, the selected and third intermediate output signals being provided as data inputs to the master and slave latches respectively;

a second control circuit coupled to the pair of master-slave latches for providing each of the master and slave latches with a set and a reset value; and

a second selector coupled to the truth table and the master-slave latches for selecting either the first, second or third intermediate output signal as the output signal of the LE.

7. The integrated circuit as set forth in claim 6, wherein each LE further comprises a buffer coupled to the second selector for outputting the output signal of the LE onto the context bus.

8. The integrated circuit as set forth in claim 6, wherein the second control circuit comprises a first and a second AND gate for receiving a first and a second plurality of input control signals, and in response, generating the set and reset values for the master and slave latches respectively.

9. The integrated circuit as set forth in claim 6, wherein the LE further comprises a third selector for selectively providing either an emulation clock or a debugging clock to the master and slave latches.

10. The integrated circuit as set forth in claim 9, wherein the LE further comprises a fourth and a fifth selector for selectively providing one of a plurality of clocks to the third selector as the emulation clock.

11. The integrated circuit as set forth in claim 5, wherein the first control circuit comprises an OR gate and an AND gate serially coupled to the OR gate for receiving a plurality of input control signals, and in response, generating an output control signal for causing the first selector to select the output signal of the LE fedback to the first selector.

12. The integrated circuit as set forth in claim 5, wherein the first control circuit comprises a NOR gate for receiving a plurality of input control signals, and in response generating an output control signal for causing the first selector to select the first intermediate output signal.

13. The integrated circuit as set forth in claim 5, wherein the control circuit receives a load control signal, and in response, output the load control signal for the first selector for causing the first selector to select the predesignated bus signal on the context bus.

14. A single integrated circuit comprising a plurality of logic elements (LEs) for generating a plurality of output signals in response to a plurality of input signals correspondingly applied to the LEs, and a scan register coupled to the LEs for serially capturing and outputting a trace record of all signal state values of the LEs in a particular clock cycle of an operating clock outside the integrated circuit, the scan register being provided with a scan clock appropriately scaled to the operating clock.

15. The integrated circuit as set forth in claim 14, wherein the integrated circuit further comprises trigger circuitry coupled to the LEs for conditionally generating at least one trigger value depending on the signal state values of the LEs.

16. The integrated circuit as set forth in claim 15, wherein the trigger circuitry comprises

a first register for storing a first trigger pattern; and

a first comparator coupled to the LEs the first register for conditionally generating a first trigger value if signal state values of the LEs match the stored first trigger pattern.

17. The integrated circuit as set forth in claim 14, wherein

each LE further includes a multiple input-single output truth table for generating a first intermediate output signal in response to a first set of input signals;

a first selector coupled to the truth table and the context bus for selecting either the first intermediate output signal, or the output of the LE fedback to the first selector, and outputting the selected signal; and

a first control circuit coupled to the first selector for controlling the first selector.

18. The integrated circuit as set forth in claims 17, wherein each LE further comprises

a pair of master-slave latches, each having a data input, a set input, and a reset input, coupled to the first selector for generating a second and a third intermediate output signal in response to the data, set, and reset inputs, the selected and third intermediate output signals being provided as data inputs to the master and slave latches respectively;

a second control circuit coupled to the pair of master-slave latches for providing each of the master and slave latches with a set and a reset value; and

a second selector coupled to the truth table and the master-slave latches for selecting either the first, second or third intermediate output signal as the output signal of the LE.

19. The integrated circuit as set forth in claim 18, wherein the LE further comprises a third selector for selectively providing either an emulation clock or a debugging clock to the master and slave latches.

20. A single integrated circuit comprising a plurality of logic elements (LEs) for generating a plurality of output signals in response to a plurality of input signals correspondingly applied to the LEs, and trigger circuitry coupled to the LEs for

conditionally generating at least one trigger value depending on the signal state values of the LEs.

21. The integrated circuit as set forth in claim 20, wherein the trigger circuitry comprises

a first register for storing a first trigger pattern; and

a first comparator coupled to the LEs the first register for conditionally generating a first trigger value if signal state values of the LEs match the stored first trigger pattern.

22. The integrated circuit as set forth in claim 20, wherein

each LE further includes a multiple input-single output truth table for generating a first intermediate output signal in response to a first set of input signals;

a first selector coupled to the truth table and the context bus for selecting either the first intermediate output signal, or the output of the LE fedback to the first selector, and outputting the selected signal; and

a first control circuit coupled to the first selector for controlling the first selector.

23. The integrated circuit as set forth in claims 22, wherein each LE further comprises

a pair of master-slave latches, each having a data input, a set input, and a reset input, coupled to the first selector for generating a second and a third intermediate output signal in response to the data, set, and reset inputs, the selected and third intermediate output signals being provided as data inputs to the master and slave latches respectively;

a second control circuit coupled to the pair of master-slave latches for providing each of the master and slave latches with a set and a reset value; and

a second selector coupled to the truth table and the master-slave latches for selecting either the first, second or third intermediate output signal as the output signal of the LE.

24. The integrated circuit as set forth in claim 23, wherein the LE further comprises a third selector for selectively providing either an emulation clock or a debugging clock to the master and slave latches.

25. A single integrated circuit comprising a plurality of logic elements (LEs) for generating a plurality of output signals in response to a plurality of input signals correspondingly applied to the LEs, each LE includes

a multiple input-single output truth table for generating a first intermediate output signal in response to a first set of input signals;

a first selector coupled to the truth table and the context bus for selecting either the first intermediate output signal, or the output of the LE fedback to the first selector, and outputting the selected signal; and

a first control circuit coupled to the first selector for controlling the first selector.

26. The integrated circuit as set forth in claims 25, wherein each LE further comprises

a pair of master-slave latches, each having a data input, a set input, and a reset input, coupled to the first selector for generating a second and a third intermediate output signal in response to the data, set, and reset inputs, the

selected and third intermediate output signals being provided as data inputs to the master and slave latches respectively;

a second control circuit coupled to the pair of master-slave latches for providing each of the master and slave latches with a set and a reset value; and

a second selector coupled to the truth table and the master-slave latches for selecting either the first, second or third intermediate output signal as the output signal of the LE.

27. The integrated circuit as set forth in claim 26, wherein the LE further comprises a third selector for selectively providing either an emulation clock or a debugging clock to the master and slave latches.